Title (en)

Method and system for driving multiple latching relays

Title (de)

Verfahren zur Ansteuerung von mehreren bistabilen Relais

Title (fr)

Méthode et système pour la commande de plusieurs relais bistabiles

Publication

EP 0474945 B1 19960904 (EN)

Application

EP 90314400 A 19901228

Priority

- CA 2025110 A 19900912
- US 58681290 A 19900924

Abstract (en)

[origin: EP0474945A1] Multiple latching relays are driven on their first side (12) by all but one of the parallel outputs of a buffered shift register B.S.R. (11a, 11b ...). Each relay on the same B.S.R. is driven on its second side (19) by the remaining parallel output of the B.S.R. A clock signal is fed to all B.S.R.s by a line (17), and causes each B.S.R. to shift all of its information one cell on the selected hedge of the clock signal. A latch signal or blanking signal is used to prevent the B.S.R.s from outputting their information to the relays during shifting. The latch or blanking signal is fed to all B.S.R.s by a line (18). A serial data message is inputted to the first B.S.R. at its serial data input (16a) . The serial data output (15) of each B.S.R. is fed to the serial data input of the succeeding B.S.R. (e.g. 16b). The information in the serial data message is such that after the shifting of all B.S.R.s is complete the appropriate signal will be on each side of each latching relay to cause it to either change or remain unchanged, as desired. The result is that one serial data line, one clock line (17), and one latching or blanking line (18), controls all of the relays. Additional latching relays can be controlled simply by adding more B.S.R.s and sending more data down the serial data line. Shift Registers which are not internally buffered may be used in an identical fashion to B.S.R.s if suitable external buffers are used. A suitable buffer must be placed between each of the outputs (13) of each Shift Register which are connected to the first sides of the latching relays, and the first side (12) of the latching relay it is coupled with, and a suitable buffer must be placed between the remaining output (14) of each Shift Register and all of the second sides of the latching relays it is coupled with. <IMAGE>

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CPC (source: EP)

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