

Title (en)

CIRCUIT ARRANGEMENT TO COMPENSATE THE BASE CURRENT OF A TRANSISTOR

Publication

EP 0476775 A3 19921021 (DE)

Application

EP 91202376 A 19910917

Priority

DE 4029889 A 19900921

Abstract (en)

[origin: US5179356A] A circuit for the compensation of a control current of a first transistor whose main current path is arranged in series with a main current path of a second transistor between two supply voltage terminals. The arrangement includes a current mirror circuit including two transistors having a common terminal connected to the one supply voltage terminal which is coupled to the second transistor. The input terminal of the current mirror is connected to a control terminal of the second transistor and its output terminal is arranged to supply a compensation current to a control terminal of the first transistor. The circuit provides an optimum compensation for the control current of the transistor amplifier (first transistor) and even in the case of low supply voltages produces a maximal signal output swing of the first transistor by the provision of a third transistor via whose main current path the compensation current is supplied and whose control terminal is connected to a node between the main current paths of the first transistor and the second transistor.

IPC 1-7

G05F 3/26

IPC 8 full level

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CPC (source: EP US)

G05F 3/265 (2013.01 - EP US)

Citation (search report)

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- [AD] US 3714600 A 19730130 - KUIJK K, et al
- [A] US 3800239 A 19740326 - CALLAHAN M
- [A] US 4451800 A 19840529 - NISHIOKA AKIRA [JP], et al

Designated contracting state (EPC)

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