

Title (en)

SYSTEM FOR COMPOUNDING INSTRUCTIONS FOR HANDLING INSTRUCTION AND DATA STREAM FOR PROCESSOR WITH DIFFERENT ATTRIBUTES

Publication

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Application

EP 91907170 A 19910329

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Abstract (en)

[origin: WO9117495A1] A system (50) with an apparatus (70) that can be used in the compounding of instructions for CISC architectures and architectures with other attributes, including RISC. The compounding is performed before instruction execution and it results in a compound instruction program (33) that can be executed in a parallel fashion on appropriate instruction execution hardware (139-141). In particular, the proposed apparatus provides compounding capability for architectures that allow the intermingling of instructions and data, contain variable length instructions (fig. 11), and allow modifications of the instruction stream. The system provides for differing and partial reference point information. An embodiment of the proposed apparatus handles the worst-case situation when it is not known which text bytes are instructions and which are data. If some information is known, the system can be simplified. The apparatus as presented provides compounds capability for any number of instructions. The system is developed particularly for machines with a S/370 instruction set, for which a number of examples are given. A backward compounding apparatus is provided. Multiple compound units and logical ORing of sequences provides system support for more difficult organizations.

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G06F 9/3853 (2013.01); **G06F 9/3885** (2013.01)

Citation (search report)

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HU 9200024 D0 19920330; HU T60048 A 19920728; JP H04505823 A 19921008; JP H04506878 A 19921126; JP H0679273 B2 19941005;
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