Title (en)

VIDEO MEMORY SYSTEM WITH INTERMEDIATE BUFFER

Publication

EP 0482263 A3 19920826 (EN)

Application

EP 90313405 A 19901210

Priority

US 60247990 A 19901024

Abstract (en)

[origin: EP0482263A2] A video memory system is disclosed including a video memory 38, an intermediate buffer 34, a video display control unit (VDUC) 42, and a video processing means 39. The intermediate buffer 34 is disposed between an external CPU 30 and the video memory 38 to intercept the address 31, data 32, and read/write signals 33 from the CPU. For read operations, signals to the video memory 38, and the data read therefrom travel through the buffer 34 to arrive at the CPU 30. For write operations, the intermediate buffer 34 stores the address and data signals from the CPU 30. The data is later written into the video memory 38 in response to a time slot reference signal 52. <IMAGE>

IPC 1-7

G09G 1/16; G09G 5/36

IPC 8 full level

G09G 1/16 (2006.01); **G09G 5/00** (2006.01); **G09G 5/39** (2006.01)

CPC (source: EP)

G09G 5/001 (2013.01); **G09G 5/39** (2013.01); **G09G 5/393** (2013.01); G09G 2360/121 (2013.01)

Citation (search report)

- [A] US 4418343 A 19831129 - RYAN JOSEPH L [US], et al
- [X] IBM TECHNICAL DISCLOSURE BULLETIN. vol. 25, no. 3B, August 1982, NEW YORK US pages 1610 - 1611; J.P. HURST: 'Simultaneous storage of two asynchronous memories for CRT refresh'
- [A] PATENT ABSTRACTS OF JAPAN vol. 009, no. 273 (P-401)30 October 1985 & JP-A-60 117 327 (FUJI XEROX KK) 24 June 1985

Cited by

DE102008003436A1; EP0613115A3; US9879898B2; US10775092B2; US11486625B2

Designated contracting state (EPC)

DE FR GB IT

DOCDB simple family (publication)

EP 0482263 A2 19920429; **EP 0482263 A3 19920826**; CA 2031625 A1 19920425

DOCDB simple family (application)

EP 90313405 A 19901210; CA 2031625 A 19901206