Title (en)

Video system

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Videosystem

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Système vidéo

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Application

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- US 63338384 A 19840723
- US 63338484 A 19840723
- US 63338584 A 19840723
- US 63338684 A 19840723
- US 63338784 A 19840723
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Abstract (en)

[origin: EP0182454A2] The present invention is a video system which includes a data processor (1), such as a microprocessor, for processing data, a video memory (5) for storing data from the data processor corresponding to an image to be displayed, a display (11), such as a raster scan cathode ray tube, for displaying the image data stored in the video memory means, and a video system controller (3) connected to the video memory (5) for controlling the transfer of data from the video memory (5) to the display (11) and between the data processor (1) and the video memory (5). The video memory (5) is preferrably a multiport dynamic randon access memory including an addressable memory array. The video system controller (3) performs a number of functions including refresh of the dynamic random access memory, multiplexing of the various access requests of the video memory and control of the blanking interval of the display. This is accomplished by having a first portion which operates synchronously with the video memory (5) and a second portion which operates synchronously with the data processor (1). The transfer operations in the video system controller are preferrably controlled through the use of a programmable state machine which manipulates inputs in a logic array.
[origin: EP0182454A2] The video system controller (3) acts to allow contention free access of the microprocessor to the system dynamic RAM(19) and to the display memory (5). In addn. the controller generates automatically the refresh cycles required for maintaining stored data. Periodically the controller operates to load new video data to the display memory shift registers. It also provides the video syne signals and blanking signals to the video monitor. A CRT monitor (11) displays data passed to it from the microprocessor over the data bus (17) under the supervision of the system controller. The controller embodies a respective row, column address latch and X,Y address logic and acts to multiplex access requests to the video memory using a printing circuit.

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EP 0182454 A2 19860528; **EP 0182454 A3 19880323**; **EP 0182454 B1 19940202**; DE 3587744 D1 19940317; DE 3587744 T2 19940519; DE 3588173 D1 19980219; DE 3588173 T2 19980610; DE 3588174 D1 19980219; DE 3588174 T2 19980610; EP 0481534 A2 19920422; EP 0481534 A3 19920826; EP 0481534 B1 19980114; EP 0482678 A2 19920429; EP 0482678 A3 19920916; EP 0482678 B1 19980114; JP H05281934 A 19931029; JP H1091136 A 19980410

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