

Publication

EP 0486194 A3 19940126

Application

EP 91310160 A 19911104

Priority

US 61435590 A 19901115

Abstract (en)

[origin: EP0486194A2] A memory system including a circuit for receiving and serially storing a plurality of instructions and a plurality of buffer memories each including a buffer controller 800, 820 for regulating access to that buffer. Also included is a circuit 830, connected to each buffer controller and said receiving circuit, for accessing one or more of said buffers in response to a first serially stored instruction while, in response to at least one other serially stored instruction, accessing at least one remaining buffer. <IMAGE>

IPC 1-7

G06F 15/72; G06F 15/64

IPC 8 full level

G06F 12/08 (2006.01); **G06T 15/00** (2006.01)

CPC (source: EP US)

G06T 15/005 (2013.01 - EP US)

Citation (search report)

- [A] US 4442503 A 19840410 - SCHUETT DIETER [DE], et al
- [A] EP 0372185 A2 19900613 - PIXAR [US]
- [A] US 3800292 A 19740326 - CURLEY J, et al
- [A] GB 2184580 A 19870624 - MITSUBISHI ELECTRIC CORP

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Designated contracting state (EPC)

DE FR GB IT

DOCDB simple family (publication)

EP 0486194 A2 19920520; **EP 0486194 A3 19940126**; CA 2055784 A1 19920516; CA 2055784 C 19980519; JP H0652051 A 19940225; JP H087715 B2 19960129; US 5511154 A 19960423

DOCDB simple family (application)

EP 91310160 A 19911104; CA 2055784 A 19911022; JP 23108891 A 19910820; US 31366894 A 19940927