

Title (en)

A digital quadrature phase detection circuit.

Title (de)

Eine digitale Schaltung zur Quadraturphasenfeststellung.

Title (fr)

Un circuit numérique de détection de phase en quadrature.

Publication

**EP 0488624 A2 19920603 (EN)**

Application

**EP 91310833 A 19911125**

Priority

JP 31862890 A 19901124

Abstract (en)

An analog quadrature-modulated signal is converted into a digital signal by an A/D converter (1) using a sampling clock having a frequency four times higher than the carrier of the quadrature modulated signal. The digital signal is delayed by one sampling slot in each of four delay circuits (2-5) connected in series to the A/D converter. The output of the A/D converter and that of the fourth delay circuit are multiplied by -1/2 by respective digital weighting circuits (6,7), and the multiplied outputs together with the output of the second delay circuit are added together in an adder (8) to generate an I component (in-phase) signal. The output of the first delay circuit is multiplied by -1 by another weighting circuit (10) and this multiplied output and the output of the third delay circuit are added together in another adder (11) to generate a Q component (quadrature phase) signal. The I and Q signals are held in latches (9,12) clocked at one quarter of the sampling clock rate. <IMAGE>

IPC 1-7

**H04L 27/22**

IPC 8 full level

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