

Title (en)  
Interprocessor switching network

Title (de)  
Vermittlungsnetz für Prozessoren

Title (fr)  
Réseau de commutation interprocesseurs

Publication  
**EP 0507044 B1 19990421 (EN)**

Application  
**EP 92100319 A 19920110**

Priority  
US 68032791 A 19910404

Abstract (en)  
[origin: EP0507044A2] A digital switching network for providing simultaneous connections among user processors of processor-based communications equipment. The user processors act as originators and destinations of data communications packets. Packet data connections are through node controllers, which communicate with gateways, which are connected to a switching network via packet links. Control messages are communicated between node controllers, gateways, and an interchange control subsystem via various control message links. All control message processing and packet data transmissions are synchronized with a packet frame synchronization signal, and processing tasks performed by each of the network subsystems are pipelined so that they occur simultaneously. Service requests are queued in a central queue in the interchange control system. The synchronization and queueing simplify the control messages that are required to set up and release the connections. <IMAGE>

IPC 1-7  
**H04L 12/56**

IPC 8 full level  
**H04Q 11/04** (2006.01); **G06F 15/173** (2006.01); **H04L 12/56** (2006.01); **H04L 12/64** (2006.01)

CPC (source: EP US)  
**H04L 49/101** (2013.01 - EP US); **H04L 49/254** (2013.01 - EP US); **H04L 49/255** (2013.01 - EP US); **H04L 49/201** (2013.01 - EP US); **H04L 49/30** (2013.01 - EP US); **H04L 49/555** (2013.01 - EP US); **H04L 2012/563** (2013.01 - EP US)

Cited by  
US5724013A; EP0622713A3; US6882649B1; US7352741B2; US7020161B1; US7065580B1; WO0176161A1; US6975626B1; US7061929B1

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**EP 92100319 A 19920110**; AT 92100319 T 19920110; AU 8881591 A 19911203; CA 2056644 A 19911129; DE 69228960 T 19920110; JP 10914492 A 19920403; US 68032791 A 19910404