Publication
EP 0511573 A3 19940216

Application
EP 92106800 A 19920421

Priority
JP 8819791 A 19910419

Abstract (en)
[origin: EP0511573A2] (Constitution) An oscillation circuit has its frequency error stored as clock adjusting data in a memory such as EEPROm or the like during a manufacture process by using a clock timer. The clock adjusting data stored in the memory are adjusted in the adjusting sequence of the clock adjusting program, which is executed for a period of 12 hours. The fast/slow adjustments are automatically accomplished to a correct time for the constant period by the clock adjusting data adjusted in the adjusting sequence. (Effects) It is possible to reduce the number of parts, improve the flexibility for design, standardize the clock circuit, eliminate the fast/slow adjusting member, and simplify the fast/slow adjustments. <IMAGE>

IPC 1-7
G04G 3/02

IPC 8 full level
G04G 3/02 (2006.01); **G06F 1/14** (2006.01)

CPC (source: EP)
G04G 3/022 (2013.01)

Citation (search report)
- [X] EP 0253227 A1 19880120 - EM MICROELECTRONIC MARIN SA [CH]
- [A] GB 2091511 A 19820728 - CITIZEN WATCH CO LTD

Cited by
EP0691598A3; EP0683443A3; US5748570A; US6304517B1

Designated contracting state (EPC)
DE GB

DOCDB simple family (publication)
EP 0511573 A2 19921104; **EP 0511573 A3 19940216**; JP H04319694 A 19921110

DOCDB simple family (application)
EP 92106800 A 19920421; JP 8819791 A 19910419