Title (en)

BUS LOCKING FIFO MULTI-PROCESSOR COMMUNICATION SYSTEM

Publication

EP 0512993 A4 19930224 (EN)

Application

EP 90914323 A 19900820

Priority

US 47435090 A 19900202

Abstract (en)

[origin: WO9111768A1] A message transfer system for transferring message data from a master processor (1140) across a VMEbus (22) to a slave processor (1140). The message transfer system includes a FIFO (1120) interconnected to the VMEbus (22) for receiving and storing the message data transferred from the master processor (1140). The FIFO FULL state, which indicates that FIFO (1120) is unable to store message data, and generates a FIFO FULL signal (1125) to indicate the existence of the FIFO FULL state. The system further includes a means (1130) interconnected to the FIFO (1120) and the VMEbus (22) responsive to the receipt of a FIFO FULL signal (1125) from the FIFO (1125).

IPC 1-7

G06F 13/38; G06F 13/00

IPC 8 full level

G06F 13/42 (2006.01)

CPC (source: EP KR)

G06F 13/38 (2013.01 - KR); **G06F 13/4217** (2013.01 - EP)

Citation (search report)

- [Y] EP 0064818 A1 19821117 - PITNEY BOWES INC [US]
- [A] PROC. EUROPEAN COMPUTER GRAPHICS CONF., September 1989, HAMBURG, DE; pages 197 - 208 M. POTMESIL ET AL 'A Parallel Image Computer with a Distributed Frame Buffer: System Architecture and Programming'
- See references of WO 9111768A1

Designated contracting state (EPC)

AT BE CH DE DK ES FR GB IT LI LU NL SE

DOCDB simple family (publication)

WO 9111768 A1 19910808; AU 6431990 A 19910821; AU 7435294 A 19941215; CA 2074530 A1 19910803; EP 0512993 A1 19921119; EP 0512993 A4 19930224; IL 95448 A0 19910630; JP H05505478 A 19930812; KR 920704225 A 19921219

DOCDB simple family (application)

US 9004697 W 19900820; AU 6431990 A 19900820; AU 7435294 A 19940930; CA 2074530 A 19900820; EP 90914323 A 19900820; IL 9544890 A 19900821; JP 51338690 A 19900820; KR 920701854 A 19920803