Title (en)

Integrated circuit using SRAM cells.

Title (de)

Integrierte Schaltung bestehend aus SRAM-Zellen.

Title (fr)

Circuit intégré utilisant des cellules SRAM.

Publication

EP 0514095 A2 19921119 (EN)

Application

EP 92304178 A 19920508

Priority

US 70127091 A 19910516

Abstract (en)

A semiconductor memory cell has parallel gate (e.g.25). The direction of the gates is desirably chosen to minimize lithographic astigmatic effects. Thus gates of comparatively uniform width are produced and predictability of transistor performance thereby improved. An embodiment of the invention features a connection between two conductive layers (35,43) and a source/drain (15). The connection forms a node between one access transistor and one pull-down transistor. <IMAGE>

IPC 1-7

H01L 27/11

IPC 8 full level

H01L 23/528 (2006.01); **H10B 10/00** (2023.01)

CPC (source: EP KR US)

H01L 23/5283 (2013.01 - EP US); **H10B 10/00** (2023.02 - KR); **H10B 10/15** (2023.02 - EP US); H01L 2924/0002 (2013.01 - EP US)

C-Set (source: EP US)

H01L 2924/0002 + H01L 2924/00

Designated contracting state (EPC)

DE ES FR GB IT

DOCDB simple family (publication)

US 5128738 A 19920707; DE 69222973 D1 19971211; DE 69222973 T2 19980305; EP 0514095 A2 19921119; EP 0514095 A3 19921230; EP 0514095 B1 19971105; ES 2109311 T3 19980116; JP 2662144 B2 19971008; JP H05160369 A 19930625; KR 100257953 B1 20000601; KR 920022535 A 19921219; TW 198131 B 19930111

DOCDB simple family (application)

US 70127091 A 19910516; DE 69222973 T 19920508; EP 92304178 A 19920508; ES 92304178 T 19920508; JP 14789492 A 19920515; KR 920007690 A 19920507; TW 81102826 A 19920411