

Title (en)

Integrated circuit using SRAM cells.

Title (de)

Integrierte Schaltung bestehend aus SRAM-Zellen.

Title (fr)

Circuit intégré utilisant des cellules SRAM.

Publication

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Application

EP 92304178 A 19920508

Priority

US 70127091 A 19910516

Abstract (en)

A semiconductor memory cell has parallel gate (e.g.25). The direction of the gates is desirably chosen to minimize lithographic astigmatic effects. Thus gates of comparatively uniform width are produced and predictability of transistor performance thereby improved. An embodiment of the invention features a connection between two conductive layers (35,43) and a source/drain (15). The connection forms a node between one access transistor and one pull-down transistor. <IMAGE>

IPC 1-7

H01L 27/11

IPC 8 full level

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CPC (source: EP KR US)

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C-Set (source: EP US)

H01L 2924/0002 + H01L 2924/00

Designated contracting state (EPC)

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US 70127091 A 19910516; DE 69222973 T 19920508; EP 92304178 A 19920508; ES 92304178 T 19920508; JP 14789492 A 19920515; KR 920007690 A 19920507; TW 81102826 A 19920411