

Title (en)
DEMULTIPLEXER COMPRISING A THREE-STATE GATE

Title (de)
DEMULTIPLEXER MIT TRI-STATE-GATTERANORDNUNG

Title (fr)
DEMULTIPLEXEUR COMPRENANT UNE PORTE A TROIS ETATS

Publication
EP 0525168 B1 19970507 (FR)

Application
EP 92906547 A 19920211

Priority
• FR 9200116 W 19920211
• US 65549891 A 19910214

Abstract (en)
[origin: WO9215085A1] A demultiplexer (25) comprises a plurality of transistors (33, 38) with conducting links between an input terminal (31) and output nodes (32). The control electrode of each transistor (33) is connected to a line of a most significant bit (MSB) bus (34) by a first capacitive device and also to a line of a least significant bit (LSB) bus (35) by a second capacitive device. When the capacitive devices associated with the same transistor receive an activation signal at the same time, the transistor (33) turns on and the current flows from the input terminal (31) to an output node (32). Each transistor in the demultiplexer (25) thus acts as a three-state gate.

IPC 1-7
H03K 17/693; H03K 17/62; G09G 3/36

IPC 8 full level
G09G 3/20 (2006.01); **G09G 3/36** (2006.01); **H03K 17/693** (2006.01); **H03M 7/22** (2006.01)

CPC (source: EP US)
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