

Title (en)  
HIGH PERFORMANCE I/O PROCESSOR

Publication  
**EP 0525860 A3 19930421 (EN)**

Application  
**EP 92202128 A 19920711**

Priority  
US 73435991 A 19910722

Abstract (en)  
[origin: EP0525860A2] An I/O Processor includes a two channel receiver (28b) and a two channel transmitter (28c) coupled to a high speed communications channel. For the receiver a status memory, specifically a FIFO, stores structuring information that indicates the beginnings and endings of PACKETS, as well as, for each BURST of data words within a packet, an indication of the occurrence of the BURST and a length L of the BURST. Additionally, there is an indication for each BURST of the presence of any errors occurring during the BURST. A corresponding data FIFO contains only the received data words, without any structuring information. A device reads both of the FIFOs, subsequent to the reception of one or more PACKETS, so as to reconstruct the original format of the received data. For the transmitter a structure control FIFO stores the structuring information for an associated data FIFO (40c, 40d), the transmitted data being structured in accordance with the structuring information. The receiver and the transmitter each include a high speed internal data path (42a, 42b) and a lower speed data path which are coupled together during slave read and write cycles, and which are decoupled during high speed DMA cycles. <IMAGE>

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**G06F 13/28**; **G06F 13/12**

IPC 8 full level  
**G06F 13/00** (2006.01); **G06F 13/12** (2006.01); **G06F 13/28** (2006.01); **G06F 13/38** (2006.01)

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Citation (search report)  
• [X] EP 0239937 A2 19871007 - WANG LABORATORIES [US]  
• [X] EP 0226975 A2 19870701 - GEN ELECTRIC [US]  
• [Y] EUROMICRO '88: 14TH EUROMICRO SYMPOSIUM ON MICROPROCESSING AND MICROPROGRAMMING vol. 24, no. 1-5, September 1988, NORTH-HOLLAND: AMSTERDAM pages 519 - 524 G.J.M. SMIT ET AL. 'the communication processor of tumult-64'

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