Title (en)

EMITTER-COUPLED LOGIC (ECL) CIRCUIT WITH HIGH OPERATING SPEED

Publication

EP 0529674 A3 19930317 (EN)

Application

EP 92114853 A 19920831

Priority

JP 22041091 A 19910830

Abstract (en)

[origin: EP0529674A2] An emitter-coupled logic (ECL) circuit includes a differential pair of transistors (Q1,Q2) and an emitter follower output stage (Q4). A load inductor (L1) is connected to one of the differential transistors and a load resistor (RL) is connected to the other one of the differential transistors. The emitter follower output stage having an input node connected to the load resistor and an output node is connected to a constant current source formed by a current source transistor (Q5) and an inductor (L2) which is AC-coupled to the load inductor (L1) by a mutual induction effect. The pull-up and pull-down delay times of the emitter coupled logic circuit can be reduced in a wide range from a light load to a heavy load. <IMAGE>

IPC 1-7

H03K 19/013

IPC 8 full level

H03K 19/086 (2006.01); **H03K 19/013** (2006.01)

CPC (source: EP US)

H03K 19/0136 (2013.01 - EP US)

Citation (search report)

- [X] EP 0297623 A2 19890104 - BROOKTREE CORP [US]
- [X] US 3728559 A 19730417 - SPANN J, et al
- [A] FR 2553606 A1 19850419 - LABO CENT TELECOMMUNICAT [FR]
- [A] US 3502901 A 19700324 - TOMOZAWA ATSUSHI, et al
- [A] EP 0068306 A1 19830105 - HONEYWELL INF SYSTEMS [IT]

Designated contracting state (EPC)

DE FR GB

DOCDB simple family (publication)

EP 0529674 A2 19930303; **EP 0529674 A3 19930317**; JP 2998325 B2 20000111; JP H0563546 A 19930312; US 5321321 A 19940614

DOCDB simple family (application)

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