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Application
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Abstract (en)
[origin: EP0529913A2] A data processing system is provided that includes a plurality of execution units 14,16 each including independent circuits for storing (30) and executing (54) instructions. A circuit (22) is also included for providing instructions from a sequence of instructions to the execution units where each instruction is provided to only one of the execution units. The system includes a circuit for detecting when an instruction in a first execution unit must complete execution prior to execution of an instruction in a second execution unit to produce correct results. A circuit is further included, responsive to the circuit for detecting, for delaying executing the instruction in the second execution unit until the instruction in the first execution unit has completed execution. <IMAGE>

IPC 1-7
G06F 9/38

IPC 8 full level
G06F 9/38 (2006.01); **G06F 9/52** (2006.01); **G06F 15/16** (2006.01); **G06F 15/177** (2006.01); **G06F 15/80** (2006.01)

CPC (source: EP US)
G06F 9/3836 (2013.01 - EP US); **G06F 9/3885** (2013.01 - EP US); **G06F 9/3889** (2013.01 - EP US)

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