

Publication

EP 0540276 A3 19940223

Application

EP 92309796 A 19921026

Priority

US 78601991 A 19911031

Abstract (en)

[origin: EP0540276A2] A method for forming a self-aligned contact utilizes a thin insulating layer formed on the upper surface of a conductive layer. A barrier layer is deposited over the insulating layer, and gate electrodes are then defined. Sidewall spacers are formed along the vertical sidewalls of the gate electrodes. During formation of the sidewall spacers the barrier layer protects the gate electrodes. A second insulating layer is then deposited and a via is opened to the substrate. A contact can now be created by depositing conductive material into the via. <IMAGE>

IPC 1-7

H01L 21/60

IPC 8 full level

H01L 21/28 (2006.01); **H01L 21/302** (2006.01); **H01L 21/3065** (2006.01); **H01L 21/336** (2006.01); **H01L 21/60** (2006.01); **H01L 21/768** (2006.01); **H01L 23/522** (2006.01); **H01L 29/78** (2006.01)

CPC (source: EP US)

H01L 21/76897 (2013.01 - EP US)

Citation (search report)

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- [A] EP 0236123 A2 19870909 - SEIKO EPSON CORP [JP]
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EP 0540276 A2 19930505; **EP 0540276 A3 19940223**; **EP 0540276 B1 19970924**; DE 69222390 D1 19971030; DE 69222390 T2 19980319; JP H05283359 A 19931029; US 5369303 A 19941129; US 5500382 A 19960319

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EP 92309796 A 19921026; DE 69222390 T 19921026; JP 29360392 A 19921102; US 11605093 A 19930902; US 29314094 A 19940819