

Title (en)

Single-transistor electrically programmable integrated memory.

Title (de)

Elektrisch programmierbarer integrierter Eintransistorspeicher.

Title (fr)

Mémoire intégrée électriquement programmable à un seul transistor.

Publication

EP 0543703 B1 19941019 (FR)

Application

EP 92403039 A 19921110

Priority

FR 9113946 A 19911113

Abstract (en)

[origin: EP0543703A1] The invention relates to a novel electrically programmable and erasable memory cell. The cell includes a single transistor which is a floating-gate transistor, with no selection transistor. Means are provided for establishing considerable capacitive coupling between the drain (12) and the floating gate (18). The capacitive coupling between the source (10) and the floating gate is weak as is customary. Preferably, the control gate (22) only partially overlaps the floating gate (18); a semi-conducting layer (26) connected to the drain overlaps another part of the floating gate. It is this latter layer which establishes the considerable capacitive coupling according to the invention. Programming can then be carried out by Fowler Nordheim effect with the source at high impedance, that is to say with no hot-electron effect. <IMAGE>

IPC 1-7

G11C 16/04; **H01L 29/52**

IPC 8 full level

G11C 17/00 (2006.01); **G11C 16/04** (2006.01); **H01L 21/8247** (2006.01); **H01L 29/423** (2006.01); **H01L 29/788** (2006.01); **H01L 29/792** (2006.01); **H10B 69/00** (2023.01)

CPC (source: EP US)

G11C 16/0425 (2013.01 - EP US); **H01L 29/42324** (2013.01 - EP US); **H01L 29/7883** (2013.01 - EP US)

Cited by

US6414877B2; WO2004021448A1; US6903975B2; US6525968B2; US6724659B2

Designated contracting state (EPC)

DE FR GB IT

DOCDB simple family (publication)

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