

Publication

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Application

EP 93302860 A 19930414

Priority

JP 9503592 A 19920415

Abstract (en)

[origin: EP0566362A2] An automatic equalizing apparatus includes: an FIR filter (13) having tap coefficients, which includes first delay circuits (1, 2) for delaying an input signal $v(t)$; a first comparison circuit (7) for comparing an output signal (26) of the filter (13) with a specified reference level to produce a signal $a(t)$; second delay circuits (100, 101) for successively delaying a signal a_m which represents $a(m.u)$ obtained by sampling the signal $a(t)$ every period of time u thereby to produce signals a_{m-i} ; a second comparison circuit (8) for comparing the output signal (26) of the filter (13) with the comparison result signal $a(t)$ thereby to produce an error signal $e(t)$; and third delay circuits (102, 103) for successively delaying a signal e_m which represents $e(m.u)$ obtained by sampling the error signal $e(t)$ every period of time u thereby to produce signals e_{m-i} . OR gates (104, 105, 106) receive the signals a_{m-i} and e_{m-i} thereby to obtain an exclusive-OR logic of signals a_j and e_{j-k} , where the signals a_j and e_{j-k} are apart at an interval of $k.u$. Integration circuits (107, 108, 109) integrate the exclusive-OR logic of the signals a_j and e_{j-k} thereby to obtain the tap coefficients to be applied to the filter. <IMAGE>

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CPC (source: EP)

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