Title (en)
   Segmented column memory array.

Title (de)
   Speichermatrix mit segmentierten Spalten.

Title (fr)
   Réseau de mémoire à colonnes segmentées.

Publication
   EP 0580467 A2 19940126 (EN)

Application
   EP 93401631 A 19930625

Priority
   US 91971592 A 19920724

Abstract (en)
   In an array of solid-state memory cells organized into rows and segmented columns and addressable by wordlines and bit lines, a memory cell
   within a segmented column is addressable by segment-select transistors which selectively connect the memory cell's pair of bit lines via conductive
   lines running parallel to the columns to a column decode circuit. The disposition of the segment-select transistors and the conductive lines relative
   to the segmented columns enables one segment-select transistor to fit in every two or more columns. In one embodiment, the segment-select
   transistors have double the pitch of the columns while the conductive lines have the same pitch of the columns. In another embodiment, the
   segment-select transistor have four times the pitch of the columns while the conductive lines have double the pitch of the columns. This enables the
   use of larger size segment-select transistors which are necessary for passing higher currents in devices such as EPROM or flash EEPROM. Column
   segmentation effectively isolates defects to individual segments and reduces the capacitance in the source and drain of an address memory cell.
   <IMAGE>

IPC 1-7
   G11C 5/06

IPC 8 full level
   G11C 17/00 (2006.01); **G11C 5/06** (2006.01); **G11C 7/18** (2006.01); **G11C 16/04** (2006.01); **H01L 21/8247** (2006.01); **H10B 69/00** (2023.01)

CPC (source: EP US)
   G11C 5/063 (2013.01 - EP US); **G11C 7/18** (2013.01 - EP US); **G11C 16/0491** (2013.01 - EP US); **H10B 69/00** (2023.02 - EP US)

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   US6285598B1; KR100385334B1; US7471581B2; US6282145B1; US7848159B2; US9640263B2

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