

Title (en)
Semiconductor memory device

Title (de)
Halbleiterspeicheranordnung

Title (fr)
Dispositif de mémoire à semi-conducteurs

Publication
EP 0591850 B1 19981223 (EN)

Application
EP 93115830 A 19930930

Priority
JP 26238292 A 19920930

Abstract (en)
[origin: EP0591850A2] The semiconductor memory device comprises a memory array (9) and a data bus line (1) for transferring read and write data between the memory array and an input buffer (IB) and an output buffer (OB) and also transferring an information indicating read or write mode operation. The data bus line transfers the read data as a complement signal having a predetermined amplitude which is smaller than a potential difference between high and low level power source lines (7 and 8, respectively). The predetermined amplitude is defined by a first and a second impedance means (2 and 3, respectively) connected between the data bus line and a first and a second power source line (7 and 8), respectively, The first impedance means (2) is associated with a first end of the data bus line in the input-output buffer area and the second impedance means (3) is associated with a second end of the data bus line in the inner circuit area of the device. The write data is transferred via the data bus line (1) as a complement signal having a larger amplitude than that of read data. The memory array accepts the signal on the data bus line as a write data signal according to its amplitude. The memory array (9) is equipped with a write control gate for detecting the amplitude of the complement signal on the data bus line (1). <IMAGE>

IPC 1-7
G11C 7/00

IPC 8 full level
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CPC (source: EP KR US)
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Cited by
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