

Title (en)
Insulated gate bipolar transistor and manufacturing method thereof

Title (de)
Bipolarer Transistor mit isolierter Steuerelektrode und Verfahren zur Herstellung desselben

Title (fr)
Transistor bipolaire à grille isolée et méthode de fabrication correspondante

Publication
EP 0594049 B1 20020130 (EN)

Application
EP 93116565 A 19931013

Priority
• JP 28166492 A 19921020
• JP 23499293 A 19930921

Abstract (en)
[origin: EP0594049A1] In an insulated gate semiconductor device (IGBT) a buffer layer (2,21,22) is included between the semiconductor substrate (12) and the conductivity modulation layer (3). This buffer layer includes regions (22) that are very highly doped and regions (21) that are less highly doped. Injection of holes from the p-type semiconductor layer (1) to the n-type semiconductor layer (3) is attained by holes which selectively flow in a region (21) where the heavily doped n-type semiconductor region is not present. The high concentration of the holes at such a region exerts a predominant influence in the device when a collector current is small, whereby flow of the collector current is facilitated and the ON-resistance of the device is suppressed. On the other hand, when the collector current is large, under a dominantly strong influence of a fact that flow of the collector current is allowed only through the region (21) where the heavily doped n-type semiconductor region is not provided, the flow of the collector current is suppressed, and hence, the durability against destruction of the device is enhanced. A low ON-resistance and an improved durability against destruction are achieved at the same time. <IMAGE>

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IPC 8 full level
H01L 29/78 (2006.01); **H01L 21/331** (2006.01); **H01L 29/08** (2006.01); **H01L 29/739** (2006.01); **H01L 21/18** (2006.01)

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Cited by
EP0746040A1; EP0725446A1; US5925911A; FR2731841A1; EP0779662A3; DE19644504B4; US5981981A; US6271061B1; WO2004030103A1; US7361970B2; US7749876B2; US7675108B2; US8101506B2

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DOCDB simple family (application)
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