Title (en)

Dual gate JFET circuit to control threshold voltage.

Title (de)

Doppelgate-JFET Schaltung zur Steuerung von Schwellspannungen.

Title (fr)

Circuit à JFET à double grille pour commander la tension de seuil.

Publication

EP 0609009 A2 19940803 (EN)

Application

EP 94300383 A 19940119

Priority

US 1038093 A 19930128

Abstract (en)

A monolithic integrated circuit includes a plurality of dual gate junction field effect transistors. One is selected as a standard transistor and its current is passed through a first resistor. A reference current is passed through a second resistor. The two resistors are coupled to the inputs of an op-amp, the output of which is coupled to one gate of the standard transistor. The other gate of the standard transistor is supplied with a bias voltage selected to operate the transistor in the conducting mode. Thus, the standard transistor forms a negative feedback loop around the op-amp. As a result, the standard transistor will pass a current related to the reference current in a ratio determined by the ratio of the resistor values. The op-amp output can then be coupled to the other gates in all of the other transistors in the integrated circuit. Accordingly, all of the transistors will have their operating currents the same as that of the standard transistor at the same operating bias. This means that all of the transistors display the same effective threshold voltage. <IMAGE>

IPC 1-7

G05F 1/56; G05F 3/24

IPC 8 full level

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CPC (source: EP)

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