

Title (en)

Integrated circuit comprising a cascode current mirror.

Title (de)

Integrierte Schaltung mit einem Kaskadestromspiegel.

Title (fr)

Circuit intégré comportant un miroir de courant en cascade.

Publication

EP 0613072 A1 19940831 (EN)

Application

EP 94200227 A 19940207

Priority

- EP 94200227 A 19940207
- EP 93200380 A 19930212

Abstract (en)

An integrated circuit comprising a cascode current mirror and a bias stage for biasing the cascode current mirror, the cascode current mirror comprising, between an input terminal (11) and a supply voltage terminal (14), a first cascoded MOS transistor (21) and a first cascode MOS transistor (22) and, between an output terminal (12) and the supply voltage terminal (14), a second cascoded MOS transistor (23) and a second cascode MOS transistor (24). In order to obtain a minimal voltage between the output terminal (12) and the supply voltage terminal (14) the bias stage comprises a first bias current source (31) for generating a first bias current, a second bias current source (32) for generating a second bias current, a first bias MOS transistor (41) having a gate coupled to the gates of the two cascoded MOS transistors (21, 23), a source, and a drain coupled to the first supply voltage terminal (13) via the first bias current source (31), a second bias MOS transistor (42) having a gate coupled to the gates of the two cascode MOS transistors (22, 24), a source coupled to the source of the first bias MOS transistor (41), and a drain coupled to the first supply voltage terminal (13) via the second bias current source (32), and a third bias MOS transistor (43) coupled between the sources of the two bias MOS transistors (41, 42) and the second supply voltage terminal (14). <IMAGE>

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IPC 8 full level

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CPC (source: EP)

G05F 3/262 (2013.01)

Citation (search report)

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- [A] EP 0403195 A1 19901219 - INMOS LTD [GB]
- [A] US 4471292 A 19840911 - SCHENCK STEPHEN R [US], et al
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EP0730214A3; WO03015476A1; US7786803B2; US7541871B2

Designated contracting state (EPC)

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