Title (en)

Method of biasing a nonvolatile flash-EEPROM memory array.

Title (de)

Verfahren zur Vorspannung einer nichtflüchtigen Flash-EEPROM-Speicheranordnung.

Title (fr)

Méthode de polarisation d'un réseau de mémoire flash-EEPROM non-volatile.

Publication

EP 0616333 A1 19940921 (EN)

Application

EP 93830110 A 19930318

Priority

EP 93830110 A 19930318

Abstract (en)

To reduce the read and write errors caused by depleted memory array cells being turned on even when not selected, the nonselected memory cells are so biased as to present a floating terminal and a terminal at a positive voltage with respect to the substrate region. In this way, the threshold voltage of the above cells (the minimum voltage between the gate and source terminals for the cell to be turned on) increases due to the "body effect", whereby the threshold voltage depends, among other things, on the voltage drop between the cell terminal operating as the source and the substrate, and increases alongside an increase in the voltage drop. <IMAGE>

IPC 1-7

G11C 16/04; G11C 16/06

IPC 8 full level

G11C 17/00 (2006.01); **G11C 16/04** (2006.01); **G11C 16/06** (2006.01); **G11C 16/30** (2006.01); **H01L 21/8247** (2006.01); **H01L 27/115** (2006.01)

CPC (source: EP US)

G11C 16/04 (2013.01 - EP US); **G11C 16/0416** (2013.01 - EP US); **G11C 16/30** (2013.01 - EP US)

Citation (search report)

- [X] DE 4213741 A1 19921119 - HYUNDAI ELECTRONICS AMERICA [US]
- [Y] US 4972371 A 19901120 - KOMORI KAZUHIRO [JP], et al
- [A] WO 8906429 A1 19890713 - ELITE SEMICONDUCTOR & SYSTEMS [US]

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US8376237B2

Designated contracting state (EPC)

DE FR GB IT

DOCDB simple family (publication)

EP 0616333 A1 19940921; **EP 0616333 B1 19990623**; DE 69325443 D1 19990729; DE 69325443 T2 20000127; JP 3553121 B2 20040811; JP H0750398 A 19950221; US 5587946 A 19961224; US 5633822 A 19970527

DOCDB simple family (application)

EP 93830110 A 19930318; DE 69325443 T 19930318; JP 4720994 A 19940317; US 21290794 A 19940315; US 45834695 A 19950602