Title (en)

DATA TRANSMISSION DELAYING CIRCUIT USING TIME-MULTIPLEXED LATCH ENABLE SIGNALS.

Publication

EP 0640261 A4 19950405 (EN)

Application

EP 92913469 A 19920514

Priority

US 9204080 W 19920514

Abstract (en)

[origin: WO9323937A1] A digital signal phase adjustment circuit adjusts the phase of a data signal in relation to a first local clock signal having a frequency of f. Also provided is a second local clock signal with a frequency of Nf, where N is a positive integer greater than 1. An N-bit shift register (120), clocked by the second local clock signal, generates N phase signals that are enabled in rotating sequential order during non-overlapping time intervals. One of the N phase signals is selected by a multiplexer (130) and used as the enable control signal for a data sampling circuit that is clocked by the second local clock signal. The data sampling circuit samples and outputs the data signal only when the selected phase signal is enabled, thereby outputting the data signal with a selected phase relative to the first clock signal.

IPC 1-7

H04L 7/027

IPC 8 full level

H03K 5/135 (2006.01); **H03D 3/24** (2006.01); **H03L 7/00** (2006.01); **H04L 7/02** (2006.01); **H04L 7/027** (2006.01); **H04L 7/033** (2006.01)

CPC (source: EP)

H03L 7/00 (2013.01); H04L 7/0338 (2013.01)

Citation (search report)

- [XY] US 4541009 A 19850910 - ROUGEOLLE DANIEL [FR], et al
- [Y] PATENT ABSTRACTS OF JAPAN vol. 15, no. 269 (E - 1087) 9 July 1991 (1991-07-09)
- See references of WO 9323937A1

Designated contracting state (EPC)

DE GB

DOCDB simple family (publication)

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