

Title (en)

Improvements in or relating to synchronization circuits.

Title (de)

Verbesserungen in Synchronisationsschaltungen.

Title (fr)

Améliorations aux circuits de synchronisation.

Publication

EP 0644524 A1 19950322 (EN)

Application

EP 94306065 A 19940817

Priority

US 10802193 A 19930817

Abstract (en)

A method of synchronizing a data signal of a controller chip 12 to a reference clock signal of a color palette chip 12 in a video driving system 10 includes the steps of altering the reference clock signal frequency, adjusting the phase of an output clock signal from the palette chip 12 wherein the output clock signal coupled with delay from controller chip 12 produces a feedback clock signal that is synchronized with the altered reference clock signal, and latching the data signal with the feedback clock signal thereby synchronizing the data signal to the reference clock signal. <IMAGE>

IPC 1-7

G09G 5/06

IPC 8 full level

G09G 5/06 (2006.01); **G09G 5/18** (2006.01)

CPC (source: EP)

G09G 5/06 (2013.01); **G09G 5/18** (2013.01)

Citation (search report)

- [PXPA] US 5291187 A 19940301 - WOOD PAUL B [US], et al
- [A] EP 0354480 A2 19900214 - SEIKO EPSON CORP [JP]
- [A] J. KLIMEK: "Hardware für XGA", ELEKTRONIK, vol. 41, no. 19, September 1992 (1992-09-01), MUNCHEN DE, pages 72 - 76
- [A] "Programmable dot clock for video adapter", IBM TECHNICAL DISCLOSURE BULLETIN, vol. 29, no. 11, April 1987 (1987-04-01), NEW YORK US, pages 4859 - 4860

Cited by

US10771068B2

Designated contracting state (EPC)

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DOCDB simple family (publication)

EP 0644524 A1 19950322; **EP 0644524 B1 19980121**; DE 69408063 D1 19980226; DE 69408063 T2 19980610

DOCDB simple family (application)

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