

Title (en)
SEMICONDUCTOR DEVICES WITH A DOUBLE GATE.

Title (de)
HALBLEITERANORDNUNG MIT DOPPELGATE.

Title (fr)
DISPOSITIFS SEMI-CONDUCTEURS A GRILLE DOUBLE.

Publication
EP 0646289 A1 19950405 (EN)

Application
EP 93910155 A 19930415

Priority
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• GB 9208324 A 19920415

Abstract (en)
[origin: US5677550A] PCT No. PCT/GB93/00792 Sec. 371 Date Oct. 14, 1994 Sec. 102(e) Date Oct. 14, 1994 PCT Filed Apr. 15, 1993 PCT Pub. No. WO93/21659 PCT Pub. Date Oct. 28, 1993An integrated circuit arrangement comprising a pair of double-gated insulated-gate transistor devices connectible in series, the first transistor of the pair being biased by one of the gates of the device so as to be operable as a depletion-mode device whilst the second transistor of the pair is biased by one of its two gates so as to be operable as an enhancement-mode device. The separately-biasable gate electrode permits the threshold voltage of the transistors to be adjusted independently so that the device may operate as either a depletion-mode transistor or as an enhancement mode transistor.

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H01L 29/772; **H01L 27/088**

IPC 8 full level
H01L 27/08 (2006.01); **H01L 27/088** (2006.01); **H01L 29/786** (2006.01)

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H01L 27/0883 (2013.01 - EP US); **H01L 29/786** (2013.01 - KR); **H01L 29/78648** (2013.01 - EP US)

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