Title (en)

SEMICONDUCTOR DEVICES WITH A DOUBLE GATE.

Title (de)

HALBLEITERANORDNUNG MIT DOPPELGATE.

Title (fr)

DISPOSITIFS SEMI-CONDUCTEURS A GRILLE DOUBLE.

Publication

EP 0646289 A1 19950405 (EN)

Application

EP 93910155 A 19930415

Priority

- GB 9300792 W 19930415
- GB 9208324 A 19920415

Abstract (en)

[origin: US5677550A] PCT No. PCT/GB93/00792 Sec. 371 Date Oct. 14, 1994 Sec. 102(e) Date Oct. 14, 1994 PCT Filed Apr. 15, 1993 PCT Pub. No. WO93/21659 PCT Pub. Date Oct. 28, 1993An integrated circuit arrangement comprising a pair of double-gated insulated-gate transistor devices connectible in series, the first transistor of the pair being biased by one of the gates of the device so as to be operable as a depletion-mode device whilst the second transistor of the pair is biased by one of its two gates so as to be operable as an enhancement-mode device. The separately-biasable gate electrode permits the threshold voltage of the transistors to be adjusted independently so that the device may operate as either a depletion-mode transistor or as an enhancement mode transistor.

IPC 1-7

H01L 29/772; H01L 27/088

IPC 8 full level

H01L 27/08 (2006.01); **H01L 27/088** (2006.01); **H01L 29/786** (2006.01)

CPC (source: EP KR US)

H01L 27/0883 (2013.01 - EP US); **H01L 29/786** (2013.01 - KR); **H01L 29/78648** (2013.01 - EP US)

Citation (search report)

See references of WO 9321659A1

Designated contracting state (EPC)

DE FR GB

DOCDB simple family (publication)

US 5677550 A 19971014; DE 69317562 D1 19980423; DE 69317562 T2 19980709; EP 0646289 A1 19950405; EP 0646289 B1 19980318; GB 9208324 D0 19920603; JP H07505742 A 19950622; KR 950701143 A 19950220; WO 9321659 A1 19931028

DOCDB simple family (application)

US 31876794 A 19941014; DE 69317562 T 19930415; EP 93910155 A 19930415; GB 9208324 A 19920415; GB 9300792 W 19930415; JP 51813593 A 19930415; KR 19940703636 A 19941013