Title (en)

A circuit for providing a sink for majority charge carriers.

Title (de)

Schaltung zur Schaffung einer Senke für Mehrheitsladungsträger.

Title (fr)

Circuit pour produire une dissipation pour porteurs de charge majoritaires.

Publication

EP 0647894 A2 19950412 (EN)

Application

EP 94202907 A 19941007

Priority

GB 9320991 A 19931012

Abstract (en)

The first electrodes (d1 and d2) of first and second transistors (Q1 and Q2) of the same polarity are coupled to one (1) of first and second voltage supply lines (1 and 2). The second electrode (s1) of the first transistor (Q1) is coupled to the other (2) of the first and second voltage supply lines (1 and 2) by a reference current source (3) for supplying a reference current (Ir) through the first transistor (Q1) and the second electrode (s2) of the second transistor (Q2) is arranged to be coupled to the other (2) of the first and second voltage supply lines (1 and 2) by a load (RL) such that in operation of the circuit majority charge carriers flow through the first and second transistors (Q1 and Q2) in a direction away from the other (2) of the first and second voltage supply lines (1 and 2). The second transistor (Q2) has dimensions which are in a predetermined ratio with corresponding dimensions of the first transistor (Q1). An amplifying arrangement (4) has a negative input (4b) coupled to the second main electrode (s1) of the first transistor (Q1), a positive input (4a) coupled to the second main electrode (s2) of the second transistor (Q2) and an output (4c) coupled to the control electrodes (g1 and g2) of the first and second transistors (Q1 and Q2) for providing a negative feedback for causing, in use of the circuit, voltages at the positive and negative inputs (4a and 4b) of the amplifying arrangement (4) to be equal thereby causing the second transistor (Q2) to supply to the load (RL) coupled between the second main electrode (s2) of the second transistor (Q2) and the other voltage supply line (2) a current (Io) related to the reference current (Ir) in accordance with the predetermined ratio. This circuit enables a constant output current (Io) to be provided with a very high output impedance. <IMAGE>

IPC 1-7

G05F 3/26

IPC 8 full level

G05F 3/24 (2006.01); **G05F 3/26** (2006.01)

CPC (source: EP)

G05F 3/262 (2013.01)

Cited by

CN115079765A; EP0994402A1; EP1004953A1; US5977651A; EP0743586A1; FR2734378A1; US5739718A; US6194957B1

Designated contracting state (EPC)

DE FR GB IT NL

DOCDB simple family (publication)

EP 0647894 A2 19950412; GB 9320991 D0 19931201; JP H07234737 A 19950905

DOCDB simple family (application)

EP 94202907 A 19941007; GB 9320991 A 19931012; JP 24640294 A 19941012