

Title (en)

Semiconductor device with wiring pattern and method for manufacturing same.

Title (de)

Halbleiterbauelement mit Leitermuster und Verfahren zur Herstellung.

Title (fr)

Dispositif semi-conducteur avec un circuit de connexion et méthode pour sa fabrication.

Publication

EP 0647966 A1 19950412 (EN)

Application

EP 94115789 A 19941006

Priority

JP 25049393 A 19931006

Abstract (en)

A semiconductor device has a dummy pattern (5) in a region close to the functional circuit module (2). The dummy pattern is of the same material as the wiring pattern (3) and is made simultaneously with the wiring pattern. A method of manufacturing the semiconductor device has a step of simultaneous forming of a wiring pattern in a functional circuit module and a dummy wiring pattern in a region close to the functional circuit module.
<IMAGE>

IPC 1-7

H01L 21/321

IPC 8 full level

H01L 21/033 (2006.01); **H01L 21/3205** (2006.01); **H01L 21/3213** (2006.01); **H01L 23/52** (2006.01)

CPC (source: EP KR)

H01L 21/0334 (2013.01 - EP); **H01L 21/302** (2013.01 - KR); **H01L 21/32139** (2013.01 - EP)

Citation (search report)

- [X] EP 0219100 A2 19870422 - TOSHIBA KK [JP]
- [X] PATENT ABSTRACTS OF JAPAN vol. 14, no. 467 (E - 989) 11 October 1990 (1990-10-11)
- [X] PATENT ABSTRACTS OF JAPAN vol. 11, no. 117 (E - 498) 11 April 1987 (1987-04-11)
- [X] PATENT ABSTRACTS OF JAPAN vol. 12, no. 457 (E - 688) 30 November 1988 (1988-11-30)

Cited by

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Designated contracting state (EPC)

DE FR GB

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EP 0647966 A1 19950412; JP H07106327 A 19950421; KR 0155584 B1 19981201; KR 950012613 A 19950516

DOCDB simple family (application)

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