

Title (en)

BICMOS ECL-TO-CMOS LEVEL TRANSLATOR AND BUFFER.

Title (de)

BICMOS-ECL NACH CMOS PEGELUMSETZER UND PUFFERSCHALTUNG.

Title (fr)

TRADUCTEUR DE NIVEAU ECL A CMOS D'UN BICMOS ET TAMPON.

Publication

EP 0655177 A4 19970326 (EN)

Application

EP 93914239 A 19930528

Priority

- US 9305106 W 19930528
- US 92929592 A 19920813

Abstract (en)

[origin: WO9405085A1] An ECL-to-CMOS level translator and BiCMOS buffer are described. The current supplied from the first input PMOS transistor (P1) is the input current to a current mirror comprising the first and second NMOS transistors (N1 and N2). The current mirror controls the current sourcing and sinking capability of the translator. Third and fourth NMOS transistors (N3 and N4) are coupled to the first and second NMOS transistors in the current mirror and function to vary the source-to-body voltage of the first and second NMOS transistors and consequently their gain which results in increased current drive and sinking capability. The BiCMOS differential buffer of the present invention provides a differential output signal on first and second output nodes (115 and 215). It is comprised of first and second cross-coupled buffers (100B and 200B). Cross-coupling the buffers results in improved high-to-low transition times.

IPC 1-7

H03K 19/0944; **H03K 19/08**; **H03K 19/003**

IPC 8 full level

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CPC (source: EP)

H03K 19/00361 (2013.01); **H03K 19/0136** (2013.01); **H03K 19/017518** (2013.01); **H03K 19/018521** (2013.01)

Citation (search report)

- [A] US 5039886 A 19910813 - NAKAMURA KAZUYUKI [JP], et al
- [A] US 4380710 A 19830419 - COHEN PAUL B, et al
- See references of WO 9405085A1

Designated contracting state (EPC)

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DOCDB simple family (publication)

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