

Title (en)
MEMORY CIRCUIT WITH REDUNDANCY ARCHITECTURE.

Title (de)
SPEICHERSCHALTUNG MIT REDUNDANZ.

Title (fr)
CIRCUIT DE MEMOIRE AVEC REDONDANCE.

Publication
EP 0659291 A1 19950628 (FR)

Application
EP 93919413 A 19930903

Priority
• FR 9300842 W 19930903
• FR 9210695 A 19920908

Abstract (en)
[origin: FR2695493A1] Novel redundancy architecture for an integrated circuit memory. According to the invention, the redundant columns are not different from the usable columns, each usable column (except the first) serving as the redundant column for an adjacent faulty column. In practice, if a column in row j , normally designated by an output of row j of the column decoder DC, is not faulty, it will be selected by the corresponding output of the decoder DC; if, on the contrary, this column is faulty, a distant redundant column will not be used; instead, the decoder output selects the next column (row $j + 1$), which should normally have been designated by the next output (row $j + 1$) of the decoder; this next output of the decoder will be directed to a third column (row $j + 2$), and so on; the connections between the decoder outputs and the columns used will gradually thereby be shifted. The figure illustrates the memory plan in groups of $n + 1$ columns, the row decoders (DR) and column decoders (DC), the fuse circuit (CF) by means of which the faulty column is designated such that the shift in the row indicated above can be effected. By using this architecture, all the columns can be tested, even those not used.

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G06F 11/20

IPC 8 full level
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CPC (source: EP KR US)
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