

Title (en)
CONFIGURATION WITH SEVERAL ACTIVE AND PASSIVE BUS USERS

Title (de)
ANORDNUNG MIT MEHREREN AKTIVEN UND PASSIVEN BUSTEILNEHMERN

Title (fr)
AGENCEMENT REGROUPANT PLUSIEURS UTILISATEURS ACTIFS ET PASSIFS DE BUS

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Application
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Abstract (en)
[origin: US5761451A] PCT No. PCT/DE93/01042 Sec. 371 Date May 4, 1995 Sec. 102(e) Date May 4, 1995 PCT Filed Oct. 29, 1993 PCT Pub. No. WO94/10632 PCT Pub. Date May 11, 1994A system having several active (master) and passive (slave) bus users (processors), each of which is allocated a memory with its own memory area. Each bus user has read access to its own memory area and each active (master) bus user has write access to every memory area. A control line is provided for sending a control signal which indicates to the active (master) bus users accessing the memory areas whether data have already been written into the memory areas. The control signal has dominant and recessive states. Outside of the access cycles, all bus users generate a dominant state. During a cycle of access to memory areas, only the bus users in whose memory areas the data have not yet been written, generate such a signal. The system may be used in automation systems.

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