

Title (en)

FLASH MEMORY SYSTEM, AND METHODS OF CONSTRUCTING AND UTILIZING SAME.

Title (de)

FLASH-SPEICHERSYSTEM-UND VERFAHREN ZUR HERSTELLUNG UND ZUR VERWENDUNG DESSELBEN.

Title (fr)

SYSTEME DE MEMOIRE FLASH ET SES PROCEDES DE CONSTRUCTION ET D'UTILISATION.

Publication

EP 0667026 A4 19981021 (EN)

Application

EP 94900481 A 19931102

Priority

- US 9310485 W 19931102
- US 97092192 A 19921102

Abstract (en)

[origin: WO9410686A1] An N-channel SNOS or SONOS type memory array (100) has programmable memory states with a negative, depletion mode threshold lower in magnitude than the supply voltage VCC when erased and a positive threshold when programmed. During reading, the supply voltage VCC is applied to the drain (16), while a positive voltage VR less than VCC-Vds,sat is applied to the source (14), where Vds,sat is the saturation voltage of the device. A reference voltage may also be applied to the substrate (11) during a read operation. Selected devices have VR applied to the gate (12), while inhibited devices have ground or the substrate potential VSS applied to the gate (12).

IPC 1-7

G11C 11/40

IPC 8 full level

G11C 17/00 (2006.01); **G11C 11/22** (2006.01); **G11C 16/04** (2006.01); **G11C 16/26** (2006.01); **H01L 21/765** (2006.01); **H01L 21/8246** (2006.01); **H01L 21/8247** (2006.01); **H01L 27/10** (2006.01); **H01L 27/115** (2006.01); **H01L 29/788** (2006.01); **H01L 29/792** (2006.01)

CPC (source: EP KR)

G11C 16/0466 (2013.01 - EP KR); **G11C 16/16** (2013.01 - KR); **G11C 16/26** (2013.01 - EP); **H01L 21/02532** (2013.01 - KR); **H01L 21/0254** (2013.01 - KR); **H01L 21/02554** (2013.01 - KR); **H01L 21/765** (2013.01 - EP KR); **H01L 29/792** (2013.01 - EP KR); **H10B 41/30** (2023.02 - EP); **H10B 43/30** (2023.02 - EP); **H10B 69/00** (2023.02 - EP)

Citation (search report)

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- [A] US 4611308 A 19860909 - LONKY MARTIN L [US]
- [A] US 3992701 A 19761116 - ABBAS SHAKIR A, et al
- [A] PATENT ABSTRACTS OF JAPAN vol. 014, no. 179 (P - 1034) 10 April 1990 (1990-04-10)
- See references of WO 9410686A1

Designated contracting state (EPC)

DE FR GB IT NL

DOCDB simple family (publication)

WO 9410686 A1 19940511; AU 5545794 A 19940524; EP 0667026 A1 19950816; EP 0667026 A4 19981021; JP H08507411 A 19960806; KR 100354406 B1 20021226; KR 950704790 A 19951120

DOCDB simple family (application)

US 9310485 W 19931102; AU 5545794 A 19931102; EP 94900481 A 19931102; JP 51137794 A 19931102; KR 19950701733 A 19950502