Title (en)

PLL SYSTEM.

Title (de)

PLL-SYSTEM.

Title (fr)

SYSTEME ASSERVI EN PHASE.

Publication

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Application

EP 94925338 A 19940829

Priority

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Abstract (en)

[origin: WO9506359A1] The invention concerns a phase-locked loop (PLL) system, in particular a PLL system for the generation of the combination frequency for the frequency-conversion stage of an FM receiver. Series-connected to a first PLL circuit with a reference or output signal with a first, low, frequency is a second PLL circuit with a reference or output signal with a second, higher, frequency, the output signal of the first PLL circuit being fed as input to the second PLL circuit. The ratio of the output signal of the first PLL circuit to its reference signal is determined by a first frequency divider which produces, from this output signal, a signal for the phase-comparison switching of the first PLL circuit, whose frequency is decreased by an amount corresponding to the ratio determined by the first frequency divider. The ratio of the output signal of the second PLL circuit to its reference signal is determined by a second frequency divider which produces, from this output signal, a signal for the phase-comparison switching of the second PLL circuit, whose frequency is decreased by an amount corresponding to the ratio determined by the second frequency divider.

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CPC (source: EP US)

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