

Title (en)

Optimised operand formatting stage

Title (de)

Optimierte Operandformatierungsstufe

Title (fr)

Etage de formatage d'opérandes optimisé

Publication

**EP 0669572 B1 19970423 (FR)**

Application

**EP 95400366 A 19950221**

Priority

FR 9402283 A 19940228

Abstract (en)

[origin: EP0669572A1] The multiplexer has two switching units (SW1,SW2) and an inverter (I10) are connected in series between positive and negative supplies (VDD,VSS). A further inverter (I11) is connected in parallel with these units and two switching units (SW3,sw4) and inverter (I12) are also connected in parallel. Data (Da) and switching commands (Ea,Fa) are entered on input terminals (52,58,60) and the output (D'a) appears on an output terminal (56). The switching units use single P or N transistors and the invertors use pairs of single P or N transistors and the invertors use pairs of transistors in series.

IPC 1-7

**G06F 7/48; H03K 17/687; H03K 17/693**

IPC 8 full level

**G06F 7/00** (2006.01); **G06F 7/575** (2006.01); **G06F 7/76** (2006.01); **H03K 17/687** (2006.01); **H03K 17/693** (2006.01)

CPC (source: EP US)

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Designated contracting state (EPC)

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DOCDB simple family (publication)

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