Title (en)

Optimised operand formatting stage

Title (de)

Optimierte Operandformatierungsstufe

Title (fr)

Etage de formatage d'opérandes optimisé

Publication

EP 0669572 B1 19970423 (FR)

Application

EP 95400366 A 19950221

Priority

FR 9402283 A 19940228

Abstract (en)

[origin: EP0669572A1] The multiplexer has two switching units (SW1,SW2) and an invertor (I10) are connected in series between positive and negative supplies (VDD,VSS). A further invertor (I11) is connected in parallel with these units and two switching units (SW3,sw4) and invertor (I12) are also connected in parallel. Data (Da) and switching commands (Ea,Fa) are entered on input terminals (52,58,60) and the output (D'a) appears on an output terminal (56). The switching units use single P or N transistors and the invertors use pairs of single P or N transistors and the invertors use pairs of transistors in series.

IPC 1-7

G06F 7/48; H03K 17/687; H03K 17/693

IPC 8 full level

G06F 7/00 (2006.01); **G06F 7/575** (2006.01); **G06F 7/76** (2006.01); **H03K 17/687** (2006.01); **H03K 17/693** (2006.01)

CPC (source: EP US)

G06F 7/575 (2013.01 - EP US); **H03K 17/6872** (2013.01 - EP US); **H03K 17/693** (2013.01 - EP US)

Designated contracting state (EPC)

DE FR GB IT

DOCDB simple family (publication)

EP 0669572 A1 19950830; **EP 0669572 B1 19970423**; DE 69500250 D1 19970528; DE 69500250 T2 19970731; FR 2716759 A1 19950901; FR 2716759 B1 19960405; JP 3135471 B2 20010213; JP H0830433 A 19960202; US 5648925 A 19970715

DOCDB simple family (application)

EP 95400366 A 19950221; DE 69500250 T 19950221; FR 9402283 A 19940228; JP 6474395 A 19950228; US 39556495 A 19950228