

Title (en)

DATA INTEGRITY CHECK IN BUFFERED DATA TRANSMISSION.

Title (de)

NACHPRÜFUNG DER DATENINTEGRITÄT BEI GEPUFFERTER DATENÜBERTRAGUNG.

Title (fr)

CONTROLE DE L'INTEGRITE DE DONNEES LORS DE LA TRANSMISSION DE DONNEES TRANSITANT PAR UNE MEMOIRE TAMPON.

Publication

EP 0676068 A1 19951011 (DE)

Application

EP 94902778 A 19931215

Priority

- DE 4244275 A 19921228
- EP 9303572 W 19931215

Abstract (en)

[origin: US5694400A] PCT No. PCT/EP93/03572 Sec. 371 Date Aug. 10, 1995 Sec. 102(e) Date Aug. 10, 1995 PCT Filed Dec. 15, 1993 PCT Pub. No. WO94/15290 PCT Pub. Date Jul. 7, 1994Discloses a device and a method for checking by means of a checker (100). the data incorporating check bits read into a memory stack. The device comprises a first counter (20), which is connected through logical gates (30a-d) with some of the memory input lines (25), and a second counter (80) between the checker (100) and the memory (50), which is connected through logical gates (70a-d) to the memory output lines (55) corresponding to the memory input lines (25) with the first (20) and the second (80). counters generating continuous binary values. The method comprising the following stages: combination of the data to be read in with a value generated by a first counter (20) in accordance with an exclusive-OR operation; reading the logically combined data into the memory (50); reading the logically combined data from the memory (50); combination of the logically combined data read out with a value generated by a second counter (80) in accordance with an exclusive-OR operation; checking the data read out for parity in a parity checker (100). The invention may be used in a buffer memory (50) between two asynchronously timed buses.

IPC 1-7

G06F 11/10

IPC 8 full level

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CPC (source: EP US)

G06F 11/0763 (2013.01 - EP US); **G06F 11/1008** (2013.01 - EP US); **G11C 29/10** (2013.01 - EP US); **G11C 29/24** (2013.01 - EP US); **G06F 7/00** (2013.01 - EP US)

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