

Title (en)
Semiconductor device

Title (de)
Halbleitervorrichtung

Title (fr)
Dispositif semi-conducteur

Publication
EP 0689252 A1 19951227 (EN)

Application
EP 95110516 A 19910320

Priority

- EP 91302414 A 19910320
- JP 7246290 A 19900320
- JP 24915490 A 19900919
- JP 32706990 A 19901128

Abstract (en)
A semiconductor device comprises a poly-crystalline silicon layer, a dielectric layer formed on said poly-crystalline silicon layer, and a conductive layer formed on said dielectric layer. The poly-crystalline silicon layer has an uneven surface including a plurality of convex portions and a plurality of concave portions, with said convex portions being defined by growing silicon grains, such as hemispherical-like silicon grains, or mushroom-like silicon grains, projecting from the surface of the silicon layer. A typical silicon grain has a diameter in range of 30 to 170nm.

IPC 1-7
H01L 29/92

IPC 8 full level
H01L 21/02 (2006.01); **H01L 27/108** (2006.01); **H01L 29/92** (2006.01)

CPC (source: EP US)
H01L 28/84 (2013.01 - EP US); **H10B 12/318** (2023.02 - EP US); **H01L 28/82** (2013.01 - EP US); **H01L 28/90** (2013.01 - EP US);
Y10S 438/964 (2013.01 - EP US)

Citation (applicant)
"Capacitance-Enhanced Stacked-Capacitor with Engraved Storage Electrode for Deep Submicron DRAMs", SOLID STATE DEVICES AND MATERIALS, 1989, pages 137 - 140

Citation (search report)

- [X] JP S6442161 A 19890214 - HITACHI LTD
- [X] US 4742018 A 19880503 - KIMURA SHINICHIRO [JP], et al

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US9812179B2; US9679612B2; US10418091B2; US11031069B2; US10304837B2; US11081486B2

Designated contracting state (EPC)
DE FR GB

DOCDB simple family (publication)
EP 0448374 A1 19910925; EP 0448374 B1 19961023; DE 69122796 D1 19961128; DE 69122796 T2 19970220; DE 69130263 D1 19981029; DE 69130263 T2 19990218; DE 69132354 D1 20000907; DE 69132354 T2 20001228; EP 0630055 A2 19941221; EP 0630055 A3 19950104; EP 0630055 B1 19980923; EP 0689252 A1 19951227; EP 0689252 B1 20000802; KR 960012915 B1 19960925; US 5366917 A 19941122; US 5723379 A 19980303

DOCDB simple family (application)
EP 91302414 A 19910320; DE 69122796 T 19910320; DE 69130263 T 19910320; DE 69132354 T 19910320; EP 94111698 A 19910320; EP 95110516 A 19910320; KR 910004366 A 19910320; US 17799594 A 19940106; US 67207391 A 19910319