

Title (en)

DIRECT MULTILEVEL THIN-FILM TRANSISTOR PRODUCTION METHOD

Title (de)

VERFAHREN ZUR HERSTELLUNG VON NICHT-INVERTIERTEN GESTAFFELTEN DUENNSCHICHTTRANSISTOREN

Title (fr)

PROCEDE DE FABRICATION DE TRANSISTORS A COUCHES MINCES ETAGES DIRECTS

Publication

**EP 0689721 A1 19960103 (FR)**

Application

**EP 94909965 A 19940315**

Priority

- FR 9400278 W 19940315
- FR 9303012 A 19930316

Abstract (en)

[origin: WO9421102A2] A method for producing direct multilevel thin-film transistors (TFTs) with a small number of mask levels, for forming a contact between a transistor gate and the source or drain of the same or another transistor, and for use in producing flat LCD screens, particularly on screens having integral electronic control circuitry. Said method for producing direct multilevel thin-film transistors (20; 23; 24) having four mask levels comprises the steps of depositing and etching a first conductive level (11) on an insulating substrate (10) to form a source (1) and a drain (2), depositing and etching a semiconductor level (13) alone or followed by a first insulating level (16) joining the source (1) and the drain (2), depositing and etching a second insulating level (14), and depositing and etching a second conductive level (15) constituting the gate (22) of the transistor (20, 23).

IPC 1-7

**H01L 27/12; H01L 21/336; H01L 21/84**

IPC 8 full level

**G02F 1/1343** (2006.01); **G02F 1/136** (2006.01); **G02F 1/1368** (2006.01); **H01L 21/336** (2006.01); **H01L 21/77** (2006.01); **H01L 21/84** (2006.01); **H01L 27/12** (2006.01); **H01L 29/49** (2006.01); **H01L 29/786** (2006.01)

CPC (source: EP US)

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Citation (search report)

See references of WO 9421102A2

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