Title (en)

TILE BASED ARCHITECTURE FOR FPGA

Title (de)

AUS BASISMODULEN AUFGEBAUTE FPGA-ARCHITEKTUR

Title (fr)

ARCHITECTURE EN TUILES JUXTAPOSEES POUR MATRICE DE PORTES PROGRAMMABLES PAR L'UTILISATEUR

Publication

EP 0698312 A1 19960228 (EN)

Application

EP 95909504 A 19950207

Priority

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Abstract (en)

[origin: WO9522205A1] An FPGA architecture offers logic elements with direct connection to neighboring logic elements and indirect connection through a routing matrix. A logic element and a portion of the routing matrix are formed as part of a tile, and tiles are joined to form arrays of selectable size. The routing matrix includes routing lines which connect just from one tile to the next and routing lines which extend longer distances through several tiles or through the entire chip. This combination is achieved by the formation of individual tiles, all of which are identical.

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IPC 8 full level

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CPC (source: EP)

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