

Title (en)
CMOS INPUT WITH V CC? COMPENSATED DYNAMIC THRESHOLD

Title (de)
CMOS EINGANG MIT VCC-KOMPENSIERTER DYNAMISCHER SCHWELLE

Title (fr)
ENTREE DE CIRCUIT CMOS A SEUIL DYNAMIQUE COMPENSE EN V CC?

Publication
EP 0700599 B1 19980701 (EN)

Application
EP 95910702 A 19950317

Priority
• IB 9500183 W 19950317
• US 21848194 A 19940325

Abstract (en)
[origin: WO9526590A1] An inverter includes a series arrangement of a first PFET and a first NFET between Vdd and ground. The first FETs have their gates connected to one another and to the input. The inverter has a first switching threshold. A series arrangement of second and third PFETs is connected in parallel to the first PFET. The second and third PFETs are connected to Vdd and the inverter's output, respectively. A further inverter with a second switching threshold is connected to the input to control the second PFET in response to the input signal. The third PFET is controlled in parallel to the first PFET. The switching threshold of the compound circuit is substantially constant over a wide range of Vdd levels.

IPC 1-7
H03K 19/094

IPC 8 full level
H03K 19/20 (2006.01); **H03K 19/003** (2006.01); **H03K 19/0948** (2006.01)

CPC (source: EP KR US)
H03K 19/00384 (2013.01 - EP US); **H03K 19/094** (2013.01 - KR)

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• IBM Technical Disclosure Bulletin, Vol 31, No. 5, pp331-2

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