Title (en)

An apparatus and method for determining a number of digits leading a particular digit

Title (de)

Eine Vorrichtung und ein Verfahren zur Bestimmung einer Zahl von Ziffern, die einer bestimmten Ziffer vorhergehen

Title (fr)

Appareil et procédé pour déterminer un nombre de chiffres précédant un chiffre particulier

Publication

EP 0703527 A1 19960327 (EN)

Application

EP 95304950 A 19950714

Priority

US 29534794 A 19940824

Abstract (en)

When a data input signal having R plus X groups of M digits is received, the digits are segmented such that X different first counter-detectors receive M digits and a second counter-detector receives the R digits. The counter-detectors determine a number of most significant count digits leading a most significant non-count digit and detect the presence of a non-count digit. A decoder receives the outputs of the first counter-detectors and, responsive to a non-count digit detection in a most significant group of M digits having a non-count digit, communicates the corresponding count number to a concatenator. A third counter-detector determines and communicates a number of most significant groups of M digits having no non-count digits. An output of the third counter detector is concatenated with an output of the decoder where the decoder output is represented by Z digits where M=N<Z> (X, M, R, N, and Z are non-negative integers). The concatenation represents the number of leading count digits. If R is non-zero, the second counter-detector determines a number of most significant count digits leading a most significant non-count digit and detects the presence of a non-count digit in the R most significant bits. An adder then adds R to the concatenation. A multiplexer selects the number of leading count digits in the R bits if the R bits contain a non-count digit else the multiplexer selects the concatenation plus R. <IMAGE> <IMAGE>

IPC 1-7

G06F 7/00

IPC 8 full level

G06F 7/00 (2006.01); **G06F 7/74** (2006.01)

CPC (source: EP US)

G06F 7/74 (2013.01 - EP US)

Citation (applicant)

- US 5058048 A 19911015 - GUPTA SMEETA [US], et al
- US 14638293 A 19931029

Citation (search report)

- [X] US 4789956 A 19881206 - HILDEBRANDT ERIC A [US]
- [A] US 4631696 A 19861223 - SAKAMOTO TSUTOMU [JP]
- [XA] V. OKLOBDZIJA: "An Algorithmic and Novel Design of Leading Zero Detector Circuit: Comparison with Logic Synthesis", IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, vol. 2, no. 1, NEW YORK US, pages 124 - 128, XP000435270

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