

Title (en)  
METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE WITH A SEMICONDUCTOR BODY HAVING A SURFACE PROVIDED WITH A MULTILAYER WIRING STRUCTURE

Title (de)  
HERSTELLUNGSVERFAHREN FÜR EINE HALBLEITERANORDNUNG AUSGESTATTET MIT EINER HALBLEITERKÖRPEROBERFLÄCHE MIT MEHRSCICHTLEITERSTRUKTUR

Title (fr)  
PROCEDE DE FABRICATION D'UN DISPOSITIF SEMICONDUCTEUR PRESENTANT UN CORPS SEMICONDUCTEUR DOTE EN SURFACE D'UNE STRUCTURE DE CABLAGE A COUCHES MULTIPLES

Publication  
**EP 0704105 A2 19960403 (EN)**

Application  
**EP 95910699 A 19950317**

Priority  
• EP 94200940 A 19940407  
• IB 9500180 W 19950317

Abstract (en)  
[origin: WO9528000A2] A method of manufacturing a semiconductor device with a semiconductor body (2) having a surface (1) which is provided with a multilayer wiring structure (3, 9) of conductor tracks made of a same conductive material. A first wiring layer (3) comprising conductor tracks (4, 16, 18, 19, 22, 23, 24, 29, 30) is formed on the surface. These tracks are covered with an insulating layer (5, 20, 21, 25, 26, 27, 31, 32) in which contact windows (8) are formed by means of a wet etching process capable of etching the material of the insulation layer selectively relative to the conductive material, which windows expose at least a portion of the conductor tracks of the first wiring layer locally. Then a layer (10) of the conductive material is deposited on the surface, and a second wiring layer (9) of conductor tracks (11) is formed therein. Before the contact windows are formed, an auxiliary layer (12, 15) of insulating material is provided on the insulation layer. Openings (13) are etched into the auxiliary layer at the areas of the contact windows. Then the contact windows are formed in that the semiconductor body is subjected to a wet etching process capable of selectively etching the insulating material of the insulation layer not only relative to the conductive material but also relative to the insulating material of the auxiliary layer. Thanks to the use of the auxiliary layer, the conductor tracks of the second wiring layer may be made comparatively narrow.

IPC 1-7  
**H01L 21/00**

IPC 8 full level  
**H01L 21/00** (2006.01); **H01L 21/306** (2006.01); **H01L 21/768** (2006.01)

CPC (source: EP KR)  
**H01L 21/768** (2013.01 - KR); **H01L 21/76804** (2013.01 - EP); **H01L 21/76805** (2013.01 - EP); **H01L 21/76829** (2013.01 - EP)

Citation (search report)  
See references of WO 9528000A2

Designated contracting state (EPC)  
DE FR GB IT NL

DOCDB simple family (publication)  
**WO 9528000 A2 19951019**; **WO 9528000 A3 19951228**; EP 0704105 A2 19960403; JP H08511659 A 19961203; KR 100374527 B1 20030509; KR 960702940 A 19960523

DOCDB simple family (application)  
**IB 9500180 W 19950317**; EP 95910699 A 19950317; JP 52619895 A 19950317; KR 19950705487 A 19951204