

Title (en)
AN ULTRAFAST ADDER ARRANGEMENT

Title (de)
ULTRASCHNELLER ADDIERER

Title (fr)
ADDITIONNEUR ULTRARAPIDE

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Abstract (en)
[origin: WO9500900A1] A binary-lookahead-carry adder can be improved significantly by a new architecture called Distributed Binary-Lookahead-Carry (DBLC) architecture. The new architecture has truly log₂n computation levels and a very regular structure. Both the internal loading and the external loading are truly uniform and each cell is loaded by no more than two successive cells. The architecture is flexible to have single-bit or multi-bit grouped configurations in compromising speed, area and power and is suitable both for a one-clock-cycle decision and for a multi-clock-cycle pipelining. Two different versions are given, the DBLC-1 adder and the DBLC-2 adder. While the first one uses similar computation cells as that in the original binary-lookahead-carry adder, the second one uses a new computation algorithm which can give outputs of SUM and SUM +1 simultaneously. The architecture is supported by a new circuit technique called clock-and-data precharged dynamic CMOS circuit technique including both latched and non-latched versions. The circuit technique aims for a fast one-clock-cycle decision and increases speed by eliminating delay overheads of domino inverters and pipeline latches. The new adder exhibits a maximum speed, a very regular layout, a truly uniform loading and a high flexibility.

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