

Title (en)

PROCESSOR CORE WHICH PROVIDES A LINEAR EXTENSION OF AN ADDRESSABLE MEMORY SPACE

Title (de)

PROZESSORKERN MIT LINEARER ERWEITERUNG EINES SPEICHERADRESSENBEREICHES

Title (fr)

MEMOIRE CENTRALE DE PROCESSEUR A EXTENSION LINEAIRE DE L'ESPACE DE MEMOIRE ADRESSABLE

Publication

**EP 0711435 A1 19960515 (EN)**

Application

**EP 95916414 A 19950414**

Priority

- US 9504668 W 19950414
- US 24876894 A 19940525

Abstract (en)

[origin: WO9532467A1] A processor core for providing a linear extension of addressable memory space of a microprocessor with minimal additional hardware and software complexity. An N+x bit pointer register (e.g. program counter) holds an N+x bit instruction address. The N+x bit instruction address provides to an execution unit a pointer to an instruction in the memory to be processed by the execution unit. An encoder encodes the N+x bit address into an N bit encoding of the N+x bit address. The processor core can thereby address  $2^{x+1}$  times more memory locations than  $2^N$ . Two other registers each hold a portion of a data address (i.e. a pointer to a datum in memory to be operated on). An address former concatenates the portions of the address in the two registers to form the data address. Therefore, the address is formed from portions of the data address stored in multiple registers without performing any arithmetic on the portions.

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CPC (source: EP KR)

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Citation (search report)

See references of WO 9532467A1

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