

Title (en)

Circuit arrangement for generation of a regulated output voltage

Title (de)

Schaltungsanordnung zur Erzeugung einer geregelten Ausgangsspannung

Title (fr)

Circuit pour la génération d'une tension de sortie régulée

Publication

**EP 0715237 B1 20000315 (DE)**

Application

**EP 95118311 A 19951121**

Priority

DE 4442466 A 19941129

Abstract (en)

[origin: DE4442466C1] The unregulated input voltage (U) is introduced via an input connection (1) and the regulated output voltage (VDD) is tapped from an output connection (2). The load current path of a transistor (3) is connected between the input and output connections. The regulated output voltage is fed to a control amplifier (4) whose output is coupled to the transistor's control connection via a capacitor (8). The capacitor is discharged by a current source (7) controlled by the control amplifier. A charge pump (5) has an output for a raised voltage connected to the transistor's control connection and its output voltage is controlled by the control amplifier.

IPC 1-7

**G05F 1/56**

IPC 8 full level

**G05F 1/56** (2006.01)

CPC (source: EP US)

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DOCDB simple family (publication)

**DE 4442466 C1 19951214**; DE 59507999 D1 20000420; EP 0715237 A2 19960605; EP 0715237 A3 19970604; EP 0715237 B1 20000315; US 5654628 A 19970805

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