

Title (en)

PLANAR ISOLATION METHOD FOR USE IN FABRICATION OF MICROELECTRONICS

Title (de)

PLANARE ISOLATION FÜR DIE HERSTELLUNG MIKROELEKTRONISCHER ANORDNUNGEN

Title (fr)

PROCEDE D'ISOLEMENT PLANAR APTE A ETRE UTILISE DANS L'INDUSTRIE DE LA MICROELECTRONIQUE

Publication

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Application

**EP 94922567 A 19940715**

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Abstract (en)

[origin: WO9506956A1] A method of electrically isolating individual devices during the fabrication of microelectronic devices. The method is intended to replace oxide isolation methods currently used in the semiconductor industry. In a first embodiment of the present invention, the regions of a silicon substrate that are to be formed into isolation structures are exposed to a dose or doses of a noble gas implant. The noble gas implant can be preceded by a germanium implant in order to create an amorphous layer within the substrate, as a means of reducing the lateral damage caused by the noble gas implant. The noble gas implant is followed by a short time, low temperature furnace anneal which stabilizes the implanted regions. The noble gas implant suppresses epitaxial regrowth in the implanted regions, producing high resistivity and reducing leakage currents to a negligible level. In a second embodiment of the present invention, the regions of a silicon substrate that are to be formed into isolation structures are exposed to a dose or doses of germanium. The germanium implant is then followed by a short time, a low temperature furnace anneal. In either embodiment of the invention, the result is a highly effective, substantially planar isolation structure which overcomes many of the disadvantages of standard isolation techniques.

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