

Title (en)

Circuitry with gate line crossing semiconductor line at two or more channels

Title (de)

Schaltung mit Gitterzeilen, die an zwei oder mehr Kanalbereichen eine Halbleiterlinie kreuzt

Title (fr)

Circuit avec des lignes de portes croisant des lignes semiconductrices à deux ou plusieurs canals

Publication

**EP 0721214 B1 20050928 (EN)**

Application

**EP 96300049 A 19960103**

Priority

US 36798495 A 19950103

Abstract (en)

[origin: EP0721214A2] Circuitry formed at a surface of a substrate includes first and second lines (180,182) in first and second layers of the circuitry. The first line (180) includes semiconductor material and extends between first and second connecting points (190,192) at which it connects electrically to other components. The second line (182) is connected (188) to receive a gate signal, and crosses the first line (180) in two or more channel regions (184,186). The first line (180) includes a channel in each channel region, and the channels are in series. The second line (182) conducts the gate signal to all of the channel regions. The first line (180) includes charge carrier sources and destinations positioned so that conductivity of the first line between the first and second connecting points is controlled by the gate signal. The first layer can be polysilicon, and the second layer can be polysilicon or metal. The first line can be undoped in the channel regions (184,186) but heavily doped in other areas. Each of the first and second lines can include an angle of approximately 90 DEG between two of the channel regions, forming a Crossed-L configuration. In an active matrix display or other array with M scan lines and N data lines, the first line (180) can be connected to the nth data line (172) and the second line (182) can receive the gate signal from the mth scan line (170). <IMAGE>

IPC 1-7

**H01L 23/522**; H01L 23/532; G02F 1/136; H01L 27/12

IPC 8 full level

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CPC (source: EP US)

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Cited by

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