

Title (en)
Current mirror in MOS technology with adjustable cascade stages

Title (de)
Stromspiegel in MOS-Technik mit weit aussteuerbaren Kaskodestufen

Title (fr)
Miroir de courant en technologie MOS avec étages cascade réglables

Publication
EP 0730214 A3 19970716 (DE)

Application
EP 96102646 A 19960222

Priority
DE 19507155 A 19950301

Abstract (en)
[origin: EP0730214A2] The current mirror has a current bank including input and output side widely controllable cascade stages (t2,t4). A regulating circuit (r,p) generates the fixed potential of the cascade stages. A differential current (id) is fed to the control input of the regulating circuit. A first circuit node (k1) lies between a current mirror input and a first cascade stage (t2) coupled to a corresponding output of the current bank (mb). The regulation circuit includes a current controlled current source (q). The control input of the source, at a second circuit node (k2) is connected to the first node (k1). The output of the source, at a third node, is connected to a common control line (c1) for the current bank (mb). A capacitive load (c3), particularly one formed by capacitively charging the control line (c1), is connected to the third node (k3) to adjust a regulation time constant.

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G05F 3/26

IPC 8 full level
G05F 3/26 (2006.01); **H03F 3/343** (2006.01)

CPC (source: EP KR US)
G05F 3/262 (2013.01 - EP US); **H01L 23/58** (2013.01 - KR); **H01L 2924/0002** (2013.01 - EP US)

Citation (search report)
• [XA] US 4583037 A 19860415 - SOOCH NAVDEEP S [US]
• [A] EP 0606123 A1 19940713 - PHILIPS ELECTRONICS UK LTD [GB], et al
• [A] EP 0613072 A1 19940831 - PHILIPS NV [NL]
• [A] US 5099205 A 19920324 - LEWYN LANNY L [US]
• [A] US 4983929 A 19910108 - REAL PETER [US], et al

Designated contracting state (EPC)
DE FR GB IT NL

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DE 19507155 A 19950301; DE 59607907 T 19960222; EP 96102646 A 19960222; JP 4485596 A 19960301; KR 19960004758 A 19960227;
US 60814696 A 19960228