Title (en)

Process for doping two levels of a double poly bipolar transistor after formation of second poly layer

Title (de)

Verfahren zur Dotierung von zwei Ebenen eines doppel-poly-bipolaren Transistors nach Erzeugung der zweiten Poly-Ebene

Title (fr)

Procédé de dopage des deux niveaux dans un transistor bipolaire à double couche polycristalline après la formation de la seconde couche polycristalline

Publication

EP 0732746 A3 19970820 (EN)

Application

EP 96301722 A 19960313

Priority

US 40566095 A 19950317

Abstract (en)

[origin: US5686322A] A reduced mask set, implant complexity process for manufacturing a (high frequency application) complementary bipolar transistor structure uses the fast lateral diffusion characteristic of a layer of material, that is at least an order of magnitude higher for emitter dopants than in single crystal semiconductor material. Separate base and emitter poly layers are formed undoped. Then, the emitter poly of one device and the edges of the base poly of the other device are exposed through a dopant mask and simultaneously doped. The emitter dopant goes directly into the surface of the emitter poly where it lies over and is in contact with the base. The base contact dopant goes into the edges of the base poly, including the layer of material having the high diffusion coefficient, rapidly diffuses laterally throughout that layer, and then diffuses down into the collector material (e.g. island) surface, to form the extrinsic base. A second mask is patterned to expose the emitter of the second device and the edges of the base poly of the first device. Each device is then doped with the second type impurity through the second mask. The use of the high diffusion coefficient layer in the base contact enables the base dopant to spread laterally from the edge contact to the region where the base poly is in contact with the collector, with the same diffusion cycle that is used for the emitter.

IPC 1-7

H01L 27/082; H01L 21/8228

IPC 8 full level

H01L 29/73 (2006.01); **H01L 21/331** (2006.01); **H01L 21/8228** (2006.01); **H01L 27/082** (2006.01); **H01L 29/732** (2006.01)

CPC (source: EP US)

H01L 21/8228 (2013.01 - EP US); **H01L 27/082** (2013.01 - EP US); **H01L 27/0826** (2013.01 - EP US)

Citation (search report)

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- [A] EP 0445059 A2 19910904 - IBM [US]
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- [E] EP 0709894 A1 19960501 - CONS RIC MICROELETTRONICA [IT]
- [A] PATENT ABSTRACTS OF JAPAN vol. 018, no. 336 (E - 1568) 24 June 1994 (1994-06-24)

Designated contracting state (EPC)

DE FR GB IT NL

DOCDB simple family (publication)

US 5686322 A 19971111; DE 69629974 D1 20031023; DE 69629974 T2 20040722; EP 0732746 A2 19960918; EP 0732746 A3 19970820; EP 0732746 B1 20030917; JP 2008235927 A 20081002; JP 4174579 B2 20081105; JP 5076098 B2 20121121; JP H08264557 A 19961011; US 5614422 A 19970325; US 5776814 A 19980707

DOCDB simple family (application)

US 77536197 A 19970103; DE 69629974 T 19960313; EP 96301722 A 19960313; JP 2008117601 A 20080428; JP 5798596 A 19960314; US 40566095 A 19950317; US 77536097 A 19970103