

Title (en)
Reference current generator in CMOS technology

Title (de)
Referenzstromgenerator in CMOS-Technologie

Title (fr)
Générateur de courant de référence en technologie CMOS

Publication
EP 0733961 A1 19960925 (FR)

Application
EP 96400595 A 19960321

Priority
FR 9503352 A 19950322

Abstract (en)
In the current generator circuit a first current mirror (MP1,MP2) is formed with two circuit branches intended to be connected between two supply terminals (VDD,VSS). Ends of the branches comprise transistors (MP1,MN1;MP2,MN2) of opposite conductivity types connected in series. The second current mirror (MP1,MP3) generates an image (i3) of the current (i1) flowing in one of the branches. An active component (MN4) forming a variable conductance is mounted in series with the branch and is controlled in such a way that its value varies linearly with the current image (i3). This conductance thus carries a current whose strength depends solely on the technological characteristics of the active component.

Abstract (fr)
Dans ce générateur un premier miroir de courant (MP1, MP2) forme deux branches de circuit destinées à être connectées entre des bornes d'alimentation (VDD, VSS). Chacune des branches comporte des transistors (MP1, MN1; MP2, MN2) connectés en série et de types de conductivité opposés. Un second miroir de courant (MP1, MP3) engendre une image (i3) du courant (i1) circulant dans l'une des branches. Un composant actif (MN4) formant une conductance variable est montée en série cette branche et commandée de telle manière que sa valeur varie non linéairement avec l'image de courant (i3). Cette conductance est ainsi parcourue par un courant dont l'intensité dépend uniquement des caractéristiques technologiques du composant actif. <IMAGE>

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G05F 3/26; **G05F 3/24**

IPC 8 full level
G05F 3/24 (2006.01); **G05F 3/26** (2006.01)

CPC (source: EP US)
G05F 3/247 (2013.01 - EP US); **G05F 3/262** (2013.01 - EP US)

Citation (search report)
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• [A] EP 0454250 A1 19911030 - PHILIPS NV [NL]
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• [A] ERIC A. VITTOZ: "The design of High-Performance Analog Circuits on Digital CMOS Chips.", IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. 20, no. 3, NEW YORK US, pages 657 - 665, XP002005005
• [AD] ERIC A. VITTOZ: "CMOS Analog Integrated Circuits Based on Weak Inversion Operation", IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. 12, no. 3, NEW YORK US, pages 224 - 231, XP002005006

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